Parasitic Back-Gate Effect in 3-D Fully Depleted Silicon on Insulator Integrated Circuits

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***Abstract*— 3-D integrated circuits (ICs) promise to deliver faster, more compact circuitry with lower power consumption than equivalent planar ICs. However, 3-D integration introduces unique noise sources not present in planar ICs. In this paper, we identify how interconnect on a backside metal layer acts as a back gate of transistors on the adjacent tiers in 3-D fully depleted silicon on insulator technology. The resulting shift in threshold voltage is determined by process and backside interconnect geometries. We develop a framework to evaluate the impact of process parameters. Our results show that coupling due to backside metal results in 5X more electrostatic noise coupling than nearby through-oxide vias. The results also show that the change in threshold voltage of an NFET device increases with thicker front oxide, thinner buried oxide, thinner silicon film, and increased backside metal voltage. Additionally, we simulate the adverse effects of back-gate coupling on circuit performance using a representative analog test circuit, an analog amplifier. We show that the back-gate voltage can change the output of an inverting amplifier by as much as the output swing of the amplifier (0.058 V) under normal operation.**

***Index Terms*— 3-D integrated circuit (IC), back-gate effect, computer-aided design (CAD), fully depleted silicon on insulator (FDSOI).**

I. Introduction

THREE-DIMENSIONAL (3-D) integrated circuits (ICs) promise to deliver faster and more compact circuitry with lower power consumption than equivalent planar ICs [1]. It is possible to achieve 10–1000X power savings for I/O communication links and arrive at 10–1000X increase in bandwidth [2]. Many technological advances have been reported, and several demonstration systems for stacked and interposer-based integration have been announced for integrating processor and memories, analog and digital circuitry, and for FPGA-based designs [3], [4].

3-D integration, however, introduces unique noise sources that adversely affect circuit operation. Coupling between through-silicon vias and transistors via the bulk substrate has been reported [5]. Several efforts have been developed to characterize [6] and mitigate this noise source [7]. Similar coupling between through-oxide vias (TOVs) and the back gate of individual transistors in fully depleted silicon on insulator (FDSOI) 3–D ICs has been reported in [8].

In this paper, we identify a second noise source specific to 3-D FDSOI ICs—the parasitic back-gate effect due to interconnect patterned on the backside of FDSOI transistors. Here, the channel of an individual transistor is controlled not only by the front side gate-source voltage but also by metal interconnect on the adjacent tier acting as a secondary gate. Such electrostatic coupling between the front and back gates was first described by Lim and Fossum [9], who derived an analytic expression for the shift in the transistor's threshold voltage with the application of a voltage to the back gate. Their analytic expression, based on the solution to the 1-D Poisson's equation, is a function of the silicon film thickness, front oxide thickness, buried oxide thickness, and the doping density.

The analysis of the parasitic back-gate effect in 3-D circuits is complex. The back-gate effect has been previously used to control the threshold voltage variations over process tolerances, temperature, and operating requirements by directly controlling the back gate (see [10]). In 3-D ICs, the back-gate voltage of a particular transistor is, however, dependent on an interconnect signal on an adjacent tier. Depending on the layout, the backside metal pattern may not form an equipotential region under each transistor. Additionally, the back-gate potential changes independently and dynamically as a function of the global circuit, not as a local function of the particular transistor, such as found in the threshold voltage conditioning or multigate transistors.

Because parasitic back-gate coupling is unique to emerging 3-D ICs, neither computer-aided design (CAD) tools nor existing analytical formula support the compact modeling and simulation of this phenomenon. We address this deficiency with a CAD methodology based on circuit and device cosimulation. The major contributions of this paper are as follows.

1) We identify back-gate coupling as a noise source in 3-D FDSOI processes.
2) We perform the first analysis of parasitic back-gate coupling in 3-D ICs over process parameters and 3-D specific backside metal configurations.
3) We compare our simulation results with values obtained from the Lim and Fossum [9] analytic expression specifying the shift in threshold voltage due to the back-gate effect in conventional planar FDSOI transistors.
4) We provide a simulation methodology for characterizing circuit performance inclusive of parasitic back-gate coupling, at the device and circuit level. Our approach supports the complex 3-D geometries, including

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multiple, independent back-gate drivers spanning the width and length of a transistor.

5) We demonstrate the impact of parasitic back-gate coupling on a representative analog circuit, highlighting the complexity of worst-case circuit analysis.

This paper is organized as follows. In Section II, we first review the back-gate effect, including limitations in available analytical models and CAD support for noise analysis in 3-D circuits, and then summarize the MIT-LL 3-D FDSOI process. In Section III, we describe the back-gate effect in FDSOI technology. In Section IV, we present our methodology for simulating the parasitic back-gate effect in 3-D circuits. In Section V, we investigate the impact of various process parameters on the parasitic back-gate effect and compare the magnitude of this phenomenon to TOV noise coupling. In Section VI, we simulate the back-gate noise in a representative analog circuit, demonstrating the impact of parasitic back-gate coupling. We conclude our paper in Section VII with a summary and proposed future work.

II. Background and Prior Work

A. Modeling the Back-Gate Effect in FDSOI

In 1983, Lim and Fossum described how a voltage on the back gate of a FDSOI MOSFET causes a shift in its threshold voltage [9]. Since the development of the back-gate analytical equations, several improvements have been proposed. Akarvardar *et al*. [11] assumed a parabolic potential variation between the lateral junction-gates in a four gate device (G^4-FET) and analytically solved the Poisson equation. They then extended their body potential model to FDSOI MOSFETs, depicting charge-sharing and drain-induced barrier-lowing effects in short-channel devices. The accuracy of this approach relies in part on the correctness of the parabolic potential distribution assumption. Suh [12] described a compact model for both the front and back-gate threshold voltages as a closed-form expression in terms of various device geometry parameters. Suh applied bias voltages by twice updating the conventional 2-D potential expressions for the silicon body, front oxide, and BOX layers. This approximation is more efficient than the full numerical simulation, but its utility is limited to the threshold voltage modeling. The approach is not amenable to generating compact models. Wu *et al*. [13] presented a compact model of dynamically depleted silicon on insulator (SOI) MOSFETs based on reformulating the surface-potential equation to include the back-gate effect. This approach provides analytical expressions amenable to compact modeling with modest error, due primarily to the simplifying assumption of neglecting the inversion charge.

All proposed approaches above require simplifying assumptions to analytically solve the nonlinear Poisson equation. Importantly, each approach assumes that the back gate is driven by an equipotential boundary condition. While this assumption holds for devices implemented in nonstacked technologies, it does not hold for SOI devices in 3-D ICs where design rules allow multiple or partial traces to be routed under a single transistor. In this paper, we use the Synopsys TCAD tool suite to investigate the impact of the back-gate effect on SOI devices in 3-D stacked ICs.

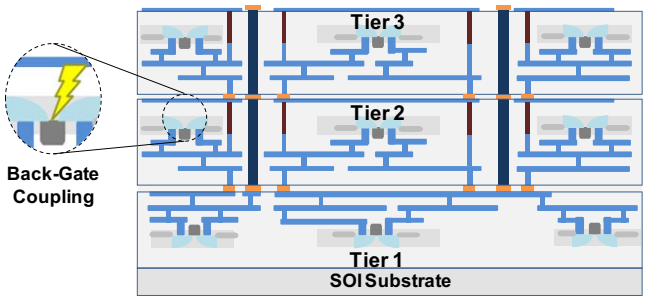

Fig. 1. MIT-LL 3-D FDSOI IC with back-gate callout.

B. MIT-Lincoln Laboratory FDSOI Process and CAD Support

A typical SOI transistor, unlike a bulk device, is fabricated in a silicon thin film grown on an oxide on a silicon handle wafer. Designers may electrically tie the substrate to a fixed potential or leave it floating. In either case, the substrate presents a constant potential to the back gate of all transistors on the wafer up to the noise processes within the substrate.

In the MIT-LL 3-D FDSOI process, the silicon handle wafer is removed and the BOX is thinned. A cap oxide is deposited on the BOX and the backside metal is patterned on the combined BOX. To achieve 3-D integration (Fig. 1), one or more independent tiers of SOI are flipped and wafer bonded to the base tier. Electrical connections are fabricated between the tiers with TOVs.

A number of MIT-LL FDSOI development processes are currently available. We focus on the 3-DM2 process, a 1.5 V, 0.18 μm 3-D process. Other active process variants include MSC2 for imager applications; 3-DM3, a 0.15-μm process; and the 090SOI12, 200HVL25, and 090XLP03 90-nm processes [14], [15]. We consider the parameters from these processes when selecting bounds on our parametric simulations. Process design kits (PDK) based on extracted device data are available from NCSU with Level 57 BSIMSOI SPICE models. While the FDSOI processes continue to evolve, existing electronic design automation support for analyzing the back-gate effect is limited. Current tools do not support the extraction of back-gate parasitics. Additionally, the BSIMSOI SPICE models do not have sufficient fidelity to simulate the back-gate effect when multiple sources contribute to the back-gate voltage.

III. Parasitic Back-Gate Effect

The parasitic back-gate effect occurs in an FDSOI process when the back side of a transistor is modulated by interconnects on an adjacent tier. More specifically, in the MIT-LL process, transistors on tier two are presented with an independent back-gate potential due to the voltages associated with the backside metal interconnect pattern (BM1), as shown in the callout in Fig. 1.

The Lim and Fossum analytical expression [9] yields the threshold voltage shift due to the back-gate voltage.

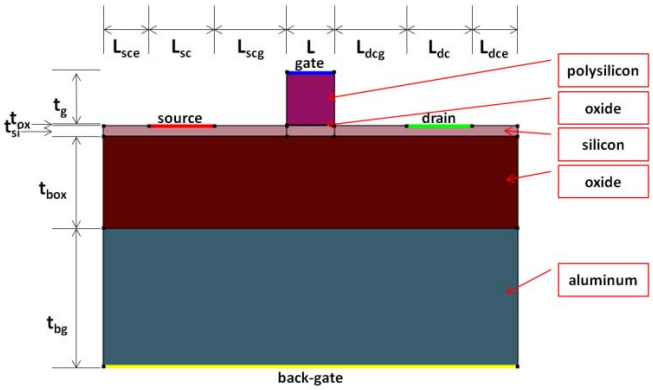

Fig. 2. Cross-section of baseline FDSOI NFET.

TABLE I
NFET BASELINE MODEL DIMENSIONS

Parameter	Description	Value
t_g	Gate thickness	200 nm
t_{ox}	Front oxide thickness	4.2 nm
t_{si}	Silicon film thickness	40 nm
t_{box}	Buried oxide thickness	345 nm
t_{bg}	Backside metal thickness	630 nm
L_{sce}	Source contact to active edge	175 nm
L_{sc}	Source contact length	250 nm
L_{scg}	Source contact to gate	275 nm
L	Transistor (channel) length	180 nm
L_{dcg}	Drain contact to gate	275 nm
L_{dc}	Drain contact length	250 nm
L_{dce}	Drain contact to active edge	175 nm

Multiple and partial traces, however, can be routed underneath a single transistor, creating multiple sources for the back-gate voltage. The back gate is no longer appropriately modeled as an equipotential region, and the Lim and Fossum expressions do not hold. The goals of this paper are to develop a methodology for analyzing this complex 3-D effect and to investigate the impact of various processing parameters (front oxide, BOX, and silicon film thicknesses) on the parasitic back-gate effect.

IV. METHODOLOGY TO MODEL THE PARASITIC BACK-GATE EFFECT IN 3-D FDSOI

Our transistor models are developed using the Synopsys TCAD tool suite. Each model is specified (geometry, material for each region, doping profiles, and contacts) with a scheme script processed by Sentaurus Structure Editor. Simple back-gate geometries, where the metal trace is under the entire width of the transistor, allow for efficient 2-D simulations. 2-D device simulations exploit device symmetry and provide results normalized to a 1-μm wide device. A user-specified factor is applied to the results to obtain a simulation of the desired transistor width. In the case of complex back-gate geometries, it was necessary to simulate the device in 3-D.

A baseline transistor model (Fig. 2) is specified with the parameters in Table I. All the values represent the default design rules associated with the 3-DM2 process, except where noted below. We simulate a minimum-size transistor with length L = 0.18 μm and width W = 0.5 μm. The BOX thickness is 345 nm, which represents the combined contribution of the nominal BOX (145 nm) and cap oxide (200 nm) between the silicon film and the backside metal. This BOX thickness corresponds with the current thinning process of record. The backside metal in the baseline model extends underneath the entire transistor. Instead of modeling the complex metal stack found in the 3-DM2 process, we utilize aluminum.

The source and drain contacts are specified per minimum process design rules: both contacts are 0.250-μm wide, with 0.275 μm spacing between the contact and the gate. There is 0.175 μm spacing between the contact and the source/drain edge. Although the physical contact cut geometry is 0.250-μm $\times$ 0.250-μm square, the model is simplified by extending the contracts along the width of the transistor to allow for 2-D simulation. All electrical contacts in the baseline model (i.e., drain, gate, source, and back gate) are modeled as 0-Ω Ohmic connections. Boundaries without contacts (e.g., the edges of the device) are modeled with ideal Neumann boundary conditions; the gradient of the electrostatic potential, polarity, and current density normal to the interface are 0 at these interfaces.

The degenerate doping profile for the silicon source and drain and the polysilicon gate is specified as a phosphorus concentration of 1.5×10^{20}/cm^3. The silicon channel is doped with a boron concentration of 5.8×10^{17}/cm^3. The doping concentrations correspond to the values extracted from the 3-DM3 process, as reflected in the NCSU 3-D PDK HSPICE models, and fall within the range of concentrations specified for the 3-DM2 process.

The model is meshed with Sentaurus Mesh, which generates axis-aligned Delaunay meshes. We experimented with various mesh densities. We iteratively refined the mesh at the interface of the silicon film and the front oxide and BOX until the computed threshold voltage difference between two successive mesh iterations was <0.003 V. The maximum mesh element length at the interfaces of the channel to the oxide layers is specified as 2 Å.

The model is simulated with Sentaurus Device, which uses numeric methods to simulate device behavior. The following physics models are included in our simulations: hydrodynamic transport models for electrons only; mobility models, including doping dependence, high field velocity saturation for holes and electrons, and transverse field dependence; Shockley-Read-Hall recombination with doping-dependent lifetime and avalanche multiplication for electrons (temperature induced) and holes (field induced); and silicon bandgap narrowing. Simulations are run on a Sunfire X4440 with four, quad core 2.3-GHz processors (AMD Opteron 8356) and 64 GB of physical memory. 2-D simulations require 15 min of CPU time per configuration, while 3-D simulations require 58.5 h of CPU time.

V. PARASITIC BACK-GATE SIMULATIONS

A. Baseline Model Characterization

We characterize the baseline transistor model, described in Section IV, by generating a set of I_D versus V_{GS} curves for

TABLE II
THRESHOLD VOLTAGE VERSUS BACK-GATE VOLTAGE

V_{bg}	V_{th} Simulated	$V_{th:}$ Lim & Fossum
0 V	0.352 V	0.351 V
1 V	0.342 V	0.339 V
2 V	0.332 V	0.327 V
3 V	0.321 V	0.315 V
4 V	0.311 V	0.304 V
5 V	0.302 V	0.292 V

the transistor and extracting the threshold voltage (Vth). The simulation is initialized by applying 0 V to all the electrical contacts and iteratively solving the Poisson equation. First the Poisson equation is solved in isolation, then again coupled with the continuity equations for electrons, and finally coupled with the continuity equations for electrons, holes, and electron temperature. After initialization, the drain voltage is ramped to 0.1 V to bias the transistor. All the voltage ramps in our simulation generate a series of quasistatic solutions by solving the fully coupled Poisson equation at each voltage step. Finally, the gate voltage is ramped to 1.5 V. The sequence is repeated for the following values for the back-gate voltage (V_{bg}): 0–5 V, 1 V steps.

The I_D versus V_{GS} curves are plotted with Synopsys Inspect, which has built in curve analysis capabilities. We use the f_VT macro to extract the threshold voltage for each curve using the extrapolation in the linear region (ELR) method [16]. This macro identifies *V*th as the V_{GS} intercept corresponding to the tangent at the maximum slope of the curve. The threshold voltage results presented are only accurate for low values of V_{DS} because we use ELR for threshold voltage extraction. For high V_{DS}, the fringing field from the drain may have more control on the channel than the underlying interconnects. A different threshold voltage extraction method is needed to accurately evaluate the impact of high V_{DS} on the back-gate effect.

The analysis results for the baseline model are shown in Table II along with the values predicted analytically by the Lim and Fossum expression. The simulated results follow the linear progression predicted by the analytical model. The threshold voltage decreases linearly with the increasing back-gate voltage. The results from the simulations and from evaluating the analytical expression are in good agreement. pMOS devices exhibit a comparable shift in the threshold voltage due to back-gate coupling.

Increasing the width of the transistor above the minimum design rule has no effect on the threshold voltage shift due to the back-gate effect. As the transistor length is, however, increased from the minimum process design rule, both the threshold voltage and the threshold voltage shift increase until they approach the theoretical values predicted by the long-channel transistor models. The threshold voltage shift with L = 0.180 μm is 0.050 V, with L = 0.360 μm is 0.058 V, and with L = 0.720 μm is 0.061 V.

B. Baseline Model Parameter Experiments

We vary three parameters, t_{box}, t_{si}, and t_{ox}, and evaluate the impact on the parasitic back-gate effect. The simulation described in Section IV is performed over the range of values listed in Table III; all the other parameters are held constant at the baseline values.

TABLE III
RANGE OF PROCESS PARAMETERS

Parameter/Configuration	Minimum	Maximum	Step
t_{box}	10 nm	610 nm	100 nm
t_{si}	5.8 nm	45.8 nm	10 nm
t_{ox}	0.72 nm	7.72 nm	1 nm

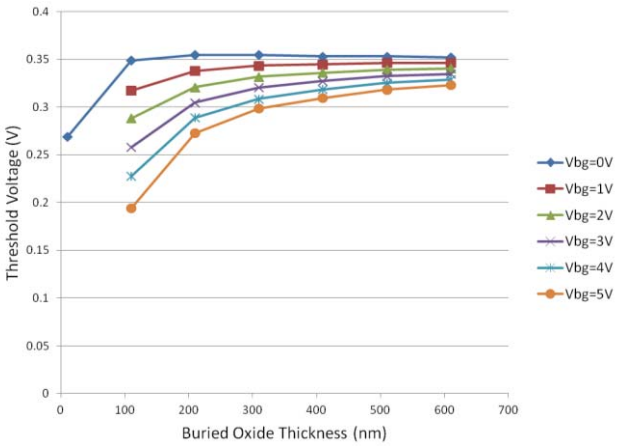

Fig. 3. Threshold voltage versus t_{box} as a function of back-gate voltage.

The parameter values on the low end are derived from the 2011 ITRS roadmap prediction for which a manufacturing solution is known [17]. The high end of the BOX thickness is set to include 600 nm, the combined BOX and cap oxide thickness for the 3-DM2 process. The high end value of the silicon film thickness is set to include 40 nm, the 3-DM2 process specification. The high end value of the front oxide thickness is set to include 7 nm, the maximum thickness available in the MCS2 process.

The results of the t_{box} parametric simulation are shown in Fig. 3. For a particular back-gate voltage, the threshold voltage decreases with a decrease in t_{box}. For thicker oxides, there is little shift in the threshold voltage across all the back-gate voltages (V_{bg} = 1, 2, …, 5 V). With thinner oxides, however, the threshold voltage shift varies considerably with increased values for the back-gate voltage. When t_{box} = 10 nm and a small positive voltage is applied to the back gate, an inversion layer is formed across the backside of the transistor, turning the device on. In this case, a negative threshold voltage is required to turn the transistor off. Data points for the 10-nm t_{box} and positive back-gate voltage are not shown in Fig. 3.

The parasitic back-gate effect increases in significance as the BOX thickness continues to decrease based on the current trends and ITRS predictions. For future 3-D ICs with very thin t_{box}, the parasitic back-gate effect will modulate transistor leakage current and may even turn transistors on and off.

The results of the t_{si} parametric simulation are shown in Fig. 4. For a particular back-gate voltage, the threshold voltage

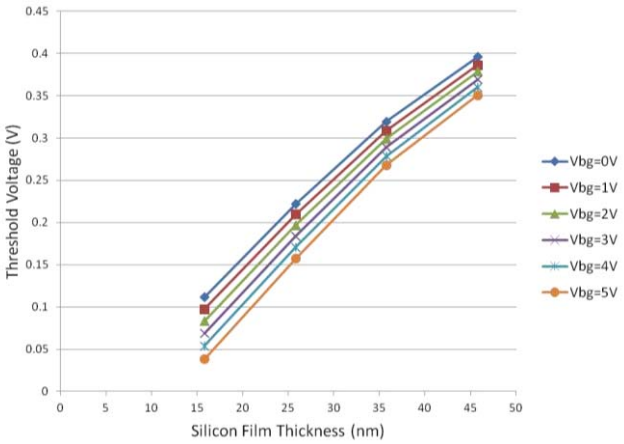

Fig. 4. Threshold voltage versus t_{si} as a function of back-gate voltage.

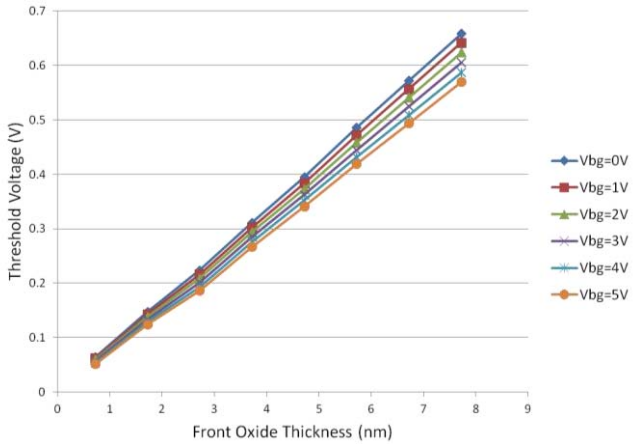

Fig. 5. Threshold voltage versus t_{ox} as a function of back-gate voltage.

decreases significantly with a decrease in t_{si}. While the range of considered silicon thickness is small, the impact of the back-gate voltage on the threshold voltage is slightly more pronounced for thinner silicon.

The parasitic back-gate effect increases in significance as t_{si} scales based on current trends and ITRS predictions. In the case of $t_{si} = 5.8$ nm (not shown in Fig. 7), with all other process parameters unchanged, the resulting transistor is a depletion mode device (i.e., the transistor is on with $V_{Gf} = 0$ V), regardless of the back-gate voltage. The ITRS roadmap for semiconductors predicts that future threshold voltages for FDSOI will be in the range of 0.219–0.332 V. Other process parameters will be modified to compensate for the dependence of Vth on t_{si}. Nevertheless, because the magnitude of the Vth dependence on the back-gate voltage increases with thinner t_{si}, noise due to the parasitic back-gate effect will likely have an increased impact on the performance of future 3-D ICs.

The results of the t_{ox} parametric simulation are shown in Fig. 5. For a particular back-gate voltage, a thinner t_{ox} results in a lower threshold voltage. The impact of the back-gate voltage on the threshold shift is more pronounced for thicker oxide thickness. As process geometries continue to scale, devices with thinner t_{ox} should be expected to exhibit reduced noise due to the parasitic back-gate effect.

The impact of the parasitic back-gate effect on the threshold voltage is highly dependent on fabrication process parameters. The Vth dependence on the back-gate voltage is increased with thinner BOX, thinner silicon film, and thicker front gate oxide. We have presented results on each parameter individually. However, the interdependence between these three parameters and other process parameters (e.g., doping profiles) must ultimately be considered together. Based on our results, while most current IC design trends lead to an increase in noise due to the parasitic back-gate effect, t_{ox} is a notable exception. However, as the ratio of t_{box} to t_{ox} approaches ten (based on ITRS predictions) from 83 (our baseline model), we anticipate that the overall impact of noise due to the parasitic back-gate effect will increase.

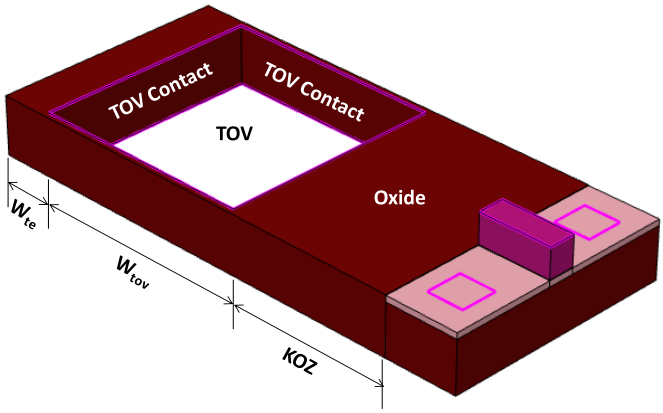

Fig. 6. Baseline transistor model with nearby TOV.

C. Noise Coupling from Backside Metal versus Nearby TOVs

To assess the magnitude of coupling due to the backside metal in comparison of noise coupling from nearby TOVs, we simulate the electrostatic noise coupling due to a nearby TOV, such as studied in [8]. The TOV is modeled as a $W_{tov} = 1.5$-μm square, located at a distance equal to the minimum keep-out zone (KOZ) of the MIT-LL process from the transistor (KOZ = 1.175 μm), as shown in Fig. 6. The TOV contact is defined as an intersecting surface between the TOV and the oxide. The width of the oxide from the TOV to the edge of the model is $W_{te} = 0.325$ μm. To isolate the coupling due to the TOV, the back-side metal was eliminated. All the other parameters and dimensions are identical to the baseline model (Table I). The voltage on the TOV is swept from 0 to 5 V.

The threshold voltage shift due to the TOV is 0.011 V. The relative magnitude of the back-gate effect on the threshold voltage shift due to the back-side metal is approximately 5X greater than the back-gate effect due to the TOV. Based on the ITRS roadmap, t_{box} will continue to decrease substantially faster than the TOV KOZ. Therefore, electrostatic back-gate coupling due to the back-side metal will dominate over similar coupling from the TOVs in current and future 3-D FDSOI circuits.

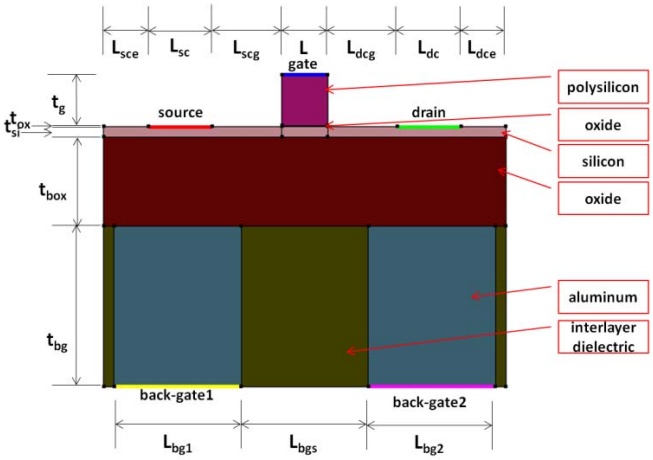

Fig. 7. Simplified NFET cross-section with two parasitic back-gate traces (widthwise configuration).

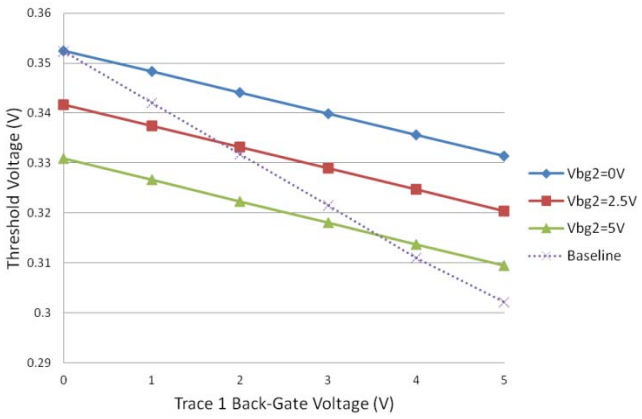

Fig. 8. Threshold voltage versus back-gate voltage (trace 1) as a function of back-gate voltage (trace 2) for the widthwise configuration in Fig. 7.

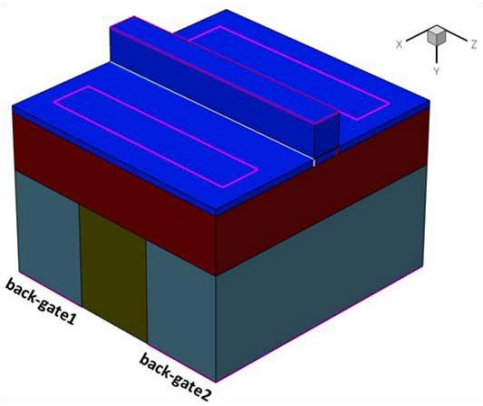

Fig. 9. Simplified 3-D NFET with two parasitic back-gate traces (lengthwise configuration). The backside aluminum traces are rotated 90° relative to the transistor topology in the widthwise configuration.

D. Experiments With Back-Gate Controlled by Multiple Sources

We introduce two additional transistor configurations, each with two traces running underneath the transistor. The transistor width is 1.5 μm to accommodate these configurations. All other dimensions are the same as shown in Table I. The first (Fig. 7) is a simplified NFET with two independent backside traces running the width of the transistor alongside the channel, separated by interlayer dielectric. This configuration is fully captured using 2-D simulations as the traces lie on the same axis as the cross-section of the drain, gate, and source. The width of the traces and their spacing are $L_{bg1} = L_{bgs} = L_{bg2} = 0.5$ μm, corresponding to the minimum 3-DM2 design rule.

One back-gate trace is ramped in steps of 2.5 V for a total of three simulation passes (0, 2.5, and 5 V). For each pass, the other back-gate trace is swept from 0–5 V.

The results are shown in Fig. 8. The threshold voltage is nearly equivalent (<0.001 V difference) when one back-gate trace is 5 V and the other is 0 V, and when both back-gate traces are 2.5 V. In addition, the $V_{bg2} = 0$ V, $V_{bg2} = 2.5$ V, and $V_{bg2} = 5$ V lines all have the same slope. Therefore, the parasitic back-gate coupling due to the two traces is linearly additive.

The results of the baseline NFET are plotted for reference (dotted line). When both the back-gate traces are 0 V, the widthwise configuration threshold voltage is equivalent to the baseline threshold voltage. The combined effect when both traces are, however, equal to 5 V (Vth = 0.309 V) is less than the baseline model (Vth = 0.302 V). The reduced back-gate effect is due to the back-gate traces being horizontally offset from the channel. The impact of the back-gate on the threshold voltage shift increases with decreasing t_{box}. The shift in threshold voltage is 0.056 V when $t_{box} = 210$ nm and 0.067 V when $t_{box} = 110$ nm.

The magnitude of the back-gate effect decreases as the separation between the backside traces is increased. With $L_{bgs} = 0.50$ μm (the minimum design rule) the threshold voltage shift is 0.043 V. With L_{bgs} increased by 50% (0.75 μm) the threshold voltage shift is reduced to 0.036 V. With L_{bgs} increased by 100% (1.00 μm) the threshold voltage shift is reduced to 0.030 V.

The second new transistor configuration (Fig. 9) is created by changing the orientation of the back-gate traces to run the length of the transistor at different positions along the width. This configuration requires full 3-D simulation because the cross-section of the drain, gate, and source is orthogonal to the cross-section of the back-gate traces. The constraint on the maximum mesh element length at the interfaces of the channel to the oxide layers is relaxed to 4 Å.

The results are shown in Fig. 10. The threshold voltage is nearly equivalent (<0.0002 V difference) when one trace is 5 V and the other is 0 V, and when both traces are 2.5 V. In addition, the traces all have the same slope. Therefore, the parasitic back-gate coupling due to the two traces is linearly additive.

The results of the baseline NFET are plotted for reference (dotted line). When both back-gate traces are 0 V, the lengthwise configuration threshold voltage is 0.003 V less than the baseline threshold voltage. The combined effect when both traces are equal to 5 V is within 0.001 V of the baseline model. The small voltage offset at these two endpoints may be due to differences in the 2-D and 3-D mesh. The impact of the back-gate on the threshold voltage shift is increased with decreasing t_{box}. The shift in threshold voltage is 0.073 V when $t_{box} = 210$ nm and 0.132 V when $t_{box} = 110$ nm.

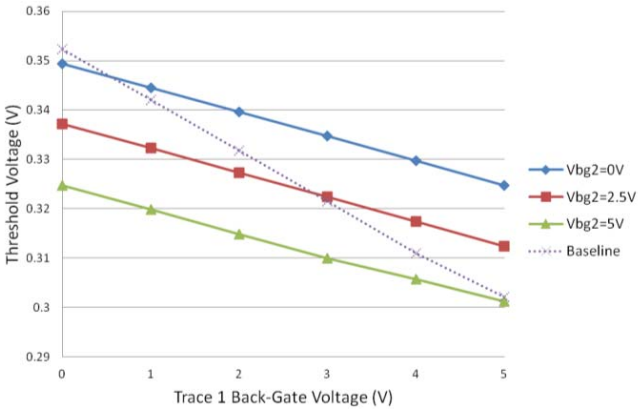

Fig. 10. Threshold voltage versus back-gate voltage (trace 1) as a function of back-gate voltage (trace 2) for the lengthwise configuration in Fig. 9.

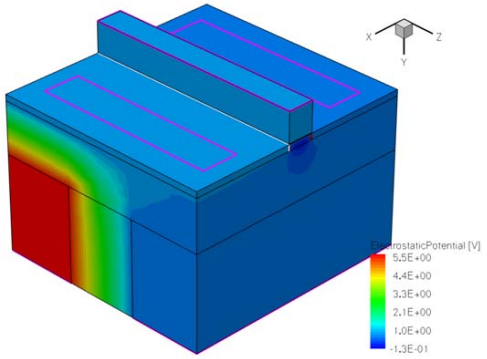

Fig. 11. Electrostatic potential plot: one back-gate trace 5 V, the other 0 V.

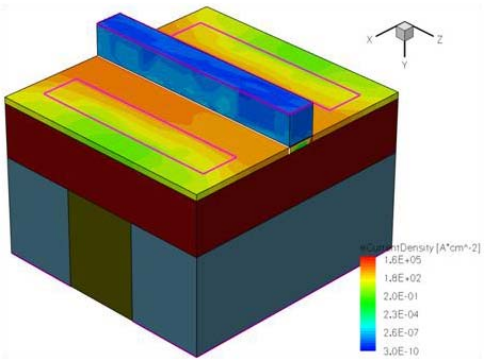

Fig. 12. Current density plot under biasing conditions stated above. There is an increase in the current density through the half of the transistor over the 5 V back-gate potential.

While the overall back-gate effect is comparable with the widthwise configuration, the effect due to each lengthwise back-gate trace is localized to half the transistor. Fig. 11 shows the electrostatic potential relative to the intrinsic Fermi level in the silicon. One back-gate trace is biased with 5 V, the other back-gate trace is biased with 0 V, the drain is biased with 0.1 V, and the gate is biased in the linear region with 0.275 V. The electrostatic potential on the transistor back gate is due to the cumulative effect of the two back-gate sources. A plot of current density (Fig. 12) shows that the transistor conducts more current across the channel on the side of the transistor over the 5 V back-gate source. This is a concrete example of a nonequipotential parasitic back gate and its effect on the operating characteristics of a transistor.

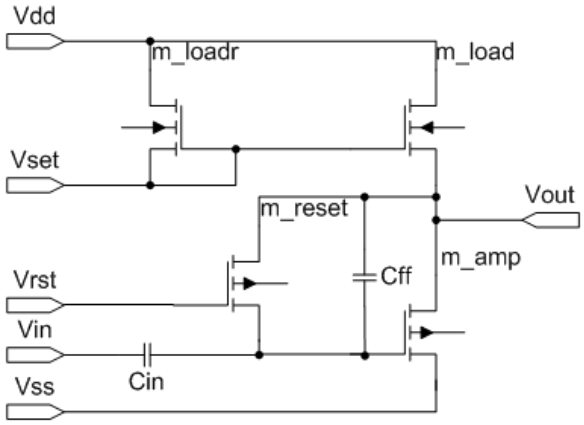

Fig. 13. Test circuit consisting of an analog FET amplifier with current mirror load. Our simulations examine the impact of applying a voltage to the back gate of individual and combinations of the transistors.

The magnitude of the back-gate effect decreases as the separation between the backside traces is increased. With $L_{bgs} = 0.50\ \mu$m (the minimum design rule) the threshold voltage shift is 0.048 V. With L_{bgs} increased by 50% (0.75 μm) the threshold voltage shift is reduced to 0.043 V. With L_{bgs} increased by 100% (1.00 μm) the threshold voltage shift is reduced to 0.038 V.

VI. Circuit Simulations

We now examine the impact of the parasitic back-gate effect on a representative analog test circuit. We simulate a common source FET amplifier with a current mirror load (Fig. 13). Amplifiers are critical components of almost all low-noise analog circuits (e.g., instrument sensors, actuators, controllers, and imager arrays). The NFETs have width W = 0.5 μm and the PFETs have width W = 1.0 μm.

The current through the primary PFET transistor of the current mirror (m_loadr) is set with an external 300-KΩ resistor (not shown) from V_{set} to ground (V_{ss}). The current through the load PFET transistor (m_load) mirrors the current though m_loadr as long as the transistors are balanced. The circuit input (V_{in}) is ac coupled to the gate of the amplifier NFET transistor (m_amp) through a 50-fF capacitor (C_{in}). A 50-fF feed-forward capacitor (C_{ff}) is placed between the gate and drain of m_amp. A reset transistor (m_reset) shunts C_{ff} when V_{rst} is high.

This circuit is an inverting amplifier; the output voltage is opposite in direction to the input voltage. When the circuit is in reset, the output settles to 0.525 V. When the circuit is released from reset and V_{in} is low (0 V), V_{out} is driven to 0.527 V. When V_{in} is high (0.1 V), V_{out} falls to 0.469 V. The total swing of V_{out} is 0.058 V around 0.498 V under normal operation.

The circuit is cosimulated (i.e., device simulation for the transistors, SPICE simulation for the circuit netlist) with Sentaurus Device. Synopsys device provides built in support for mixed-mode simulations where the physical device models are integrated as the components within a compact circuit netlist. The circuit is implemented with the baseline NFET model and a comparable PFET model. The PFET gate, source,

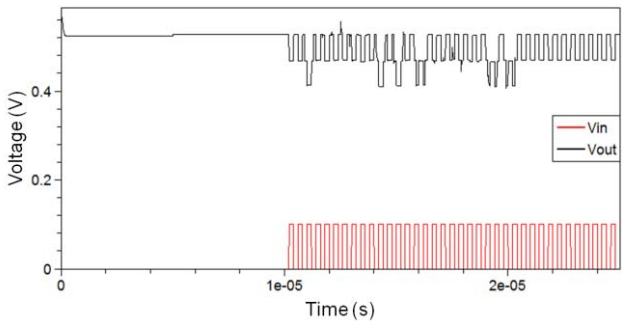

Fig. 14. Parasitic back–gate effect on Vout with various back metal traces switching between 0–5 V.

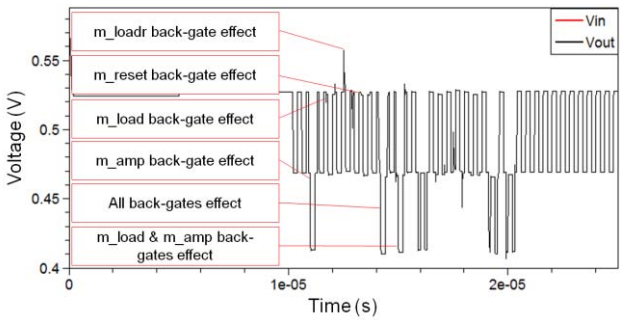

Fig. 15. Parasitic back-gate effect on Vout–zoom view.

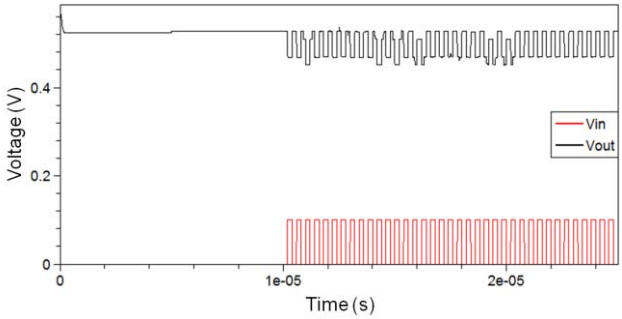

Fig. 16. Parasitic back-gate effect on Vout with various back metal traces switching between 0–1.5 V.

and drain are doped with a degenerate concentration of boron. The channel is doped with a phosphorus concentration of $6.0 \times 10^{17}/\text{cm}^3$. The hydrodynamic physics models for the PFET are based on the hole temperature instead of electron temperature. The remaining physics models are the same as those used in the baseline simulation. A 2.5-μs transient simulation is run with an initial step of 1 ns, maximum step of 100 ns, and minimum step of 1 fs. At each time increment, the Poisson equation for each transistor is solved coupled with the continuity equations for electrons and holes.

Voltage elements are used to drive the simulation. A piecewise linear voltage source is connected to V_{rst} to apply 1.5 V at time 0 with a rise time of 1 ns, and 0 V after 5 μs with a fall time of 5 ns. A pulse voltage source is connected to V_{in} with a pulse amplitude of 0.1 V, initial time delay of 10.2 μs, rise time of 5 ns, fall time of 5 ns, pulse width of 200 ns, and a period of 400 ns. V_{dd} for this circuit is 1.5 V.

The traces corresponding to the transistor back gates are driven with piecewise linear voltage sources. The back-gate signals are first switched individually and then in combination. We run two complete sets of simulations with the back-gate voltage amplitude 5 and 1.5 V, respectively. 3-D enables the vertical integration of heterogeneous layers. The MIT-LL process family includes variants optimized for 1.5 and 3.3 V logic, and supports up to 5 V operation. Therefore, voltages higher than the tier V_{dd} may drive the back gate from adjacent tiers. We selected 5 V because it is the highest voltage supported by the MIT-LL process and 5 V is often found in high-performance analog applications that leverage FDSOI technology (e.g., high sensitivity imagers). The back-gate signals are switched in the following order: m_amp, m_load, m_loadr, m_reset, none, all, m_load, and m_amp together. We repeat the entire sequence twice for each simulation: first switching the back gates when the amplifier input is low and then when the amplifier input is high.

The results of the 5 V simulation are shown in Fig. 14. The voltage applied to the back gate of each transistor has a unique effect on the circuit. A 5 V signal on the back gate of m_amp shifts the amplifier output by 0.056 V, an amount comparable with the voltage swing of the amplifier under normal operation. The back-gate effect on m_loadr and m_load unbalances the current mirror, changing the load current. This change temporarily shifts the amplifier output. The effect is more pronounced in the primary leg of the current mirror (m_loadr) (0.02 V output shift) than the secondary (m_load) (0.001 V output shift). As expected, the back gate has a negligible effect on m_reset when the circuit is out of reset.

After individually switching the back gate of each transistor, we switch all back gates simultaneously, and then those of m_load and m_amp together. The zoom view in Fig. 15 shows that particular combinations (e.g., back gate of m_load and m_amp) result in a similar total shift in the amplifier output (0.058 V) as all transistor back gates switching together (0.059 V). In the second simulation pass, where the back-gates are switched when the amplifier input is high, the back-gate effect from m_load and m_amp exceeds the effect from all the back gates switching together due to the high frequency overshoot. Because the back-gate effect of each transistor independently affects the circuit, the worst case performance does not, in general, correspond to a single backside metal voltage. Combinations of the back-gate voltages result in circuit effects that add or cancel dynamically with the circuit operation, significantly increasing the complexity required to predict the circuit performance over all possible combinations.

The results of the 1.5 V simulation are shown in Fig. 16. The primary difference between the 1.5 and the 5 V simulations is the decreased magnitude of the back-gate coupling on V_{out}.

In addition to assessing the impact of the back-gate effect on analog circuits, we also simulated a CMOS inverter with a fan-out of four. The nMOS and pMOS transistor models are the same as those used in the amplifier circuit and V_{dd} is 1.5 V. The leakage current (I_{OFF}) of the nMOS transistor is increased from $I_{OFF} = 0.154$ nA when the back-gate voltage is 0 V to $I_{OFF} = 0.261$ nA when the back-gate voltage is 1.5 V to $I_{OFF} = 0.879$ nA when the back-gate voltage is 5 V. This increase in the leakage current due to the back-gate voltage will result in substantial increase in the leakage current in large digital

circuits. The saturation current (I_{ON}) is essentially unchanged from $I_{ON} = 18.2\ \mu A$ regardless of back-gate voltage.

VII. Conclusion

We have described how a voltage applied to the back gate of a transistor in 3-D FDSOI technology can be a significant noise source. We have examined the impact of the parasitic back-gate effect on the threshold voltage and have shown that it is highly dependent on fabrication process parameters. The threshold voltage is decreased with thinner BOX, thinner silicon film, and thicker front gate oxide. We have shown that the electrostatic noise coupling from back-side metal traces is more significant than the similar coupling to TOVs. We have presented a methodology for simulating the circuit performance inclusive of the parasitic back-gate effect. Our methodology supports the simulation of multisource back-gate voltages. We have applied our methodology to analyze the parasitic back-gate effect on an example amplifier circuit. We have shown that the back-gate effect can move the amplifier output by as much as the output swing of the amplifier (0.058 V) under normal operation.

Because of its superior isolation, FDSOI is often used in high performance analog applications. Unanticipated fluctuations in transistor outputs due to back-gate transients will be disruptive. As the process parameters continue to scale, the back-gate effect will become more pronounced. While our methodology was sufficient to analyze the back-gate effect in individual transistors and for limited circuit configurations, there is a need for automated extraction of 3-D circuits inclusive of the back-gate and other 3-D specific parasitics. Additionally, there is a need for versatile compact simulation models that allow specifying complex scenarios possible with various back-gate geometries.

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